Designing with LITTLE FOOT® Power MOSFETs in Surface-Mount (SO-8) Packages

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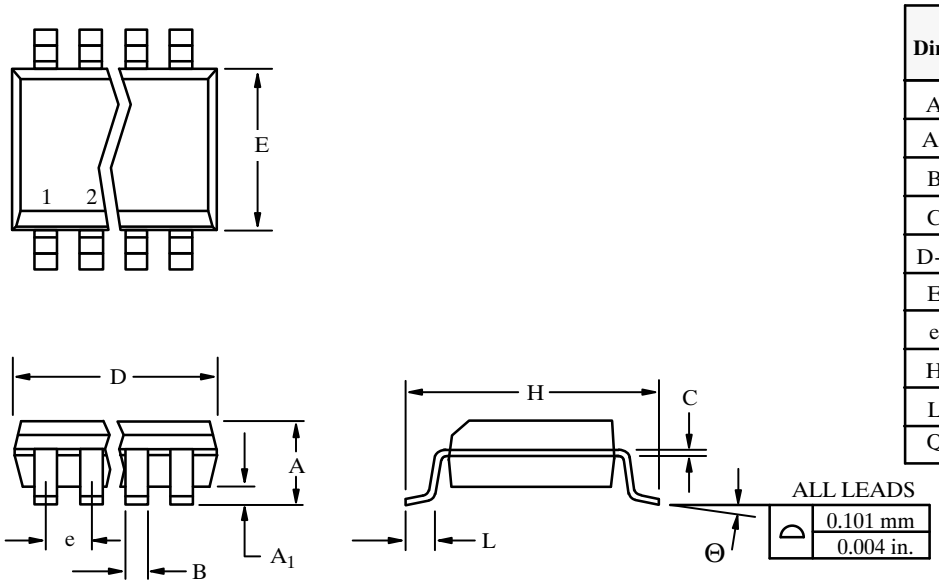
Siliconix' LITTLE FOOT power MOSFETs pack potent power handling into tiny surface-mount packages. The standard-outline, 8-pin SOIC package (Figure 1) has a copper leadframe that maximizes thermal transfer while maintaining complete compatibility with existing surface-mount technology. The complementary n- and p-channel Si9942DY LITTLE FOOT device can be used to drive inductive loads such as motors, solenoids, and relays directly, or as a low-impedance buffer to drive larger power MOSFETs or other capacitive loads.

LITTLE FOOT devices offer measurable advantages in a variety of low-voltage motor drive applications. In a computer hard disk, key features such as track density, seek time, and power consumption are directly related to the efficiency of the spindle motor and the head actuator drive circuitry. Disk drives must squeeze maximum motor performance from low-voltage supplies (traditionally, well-regulated 12-V supplies) provided by the computer system. The advent of sophisticated full-function portable computers brings new performance expectations of battery driven systems (and 5-V operation).

For 12-V battery powered applications, designers must strive to limit voltage drops—which waste motor drive voltage, reduce battery life, and contribute heat that must be dissipated, often at considerable expense. LITTLE FOOT devices such as the complementary n- and p-channel Si9942DY substantially increase the motor size that can be driven from surface-mount power devices without additional heatsinking.

The Si9942DY can also be used in power conversion applications as a buffer stage to drive highly capacitive power MOSFET gates at the high frequencies used in modern designs. For example, by using an Si9942DY to buffer the output of highly efficient CMOS PWM controllers, capacitive loads in excess of 3000 pF can be efficiently switched at rates greater than 1 MHz. This switching ability greatly extends the output power range of CMOS switchmode ICs.

This application note describes the basic MOSFET parameters that are important when driving inductive and capacitive loads and shows characteristics of the Si9942DY.



Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.53	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Q	0°	8°	0°	8°

Figure 1. LITTLE FOOT Package Dimensions

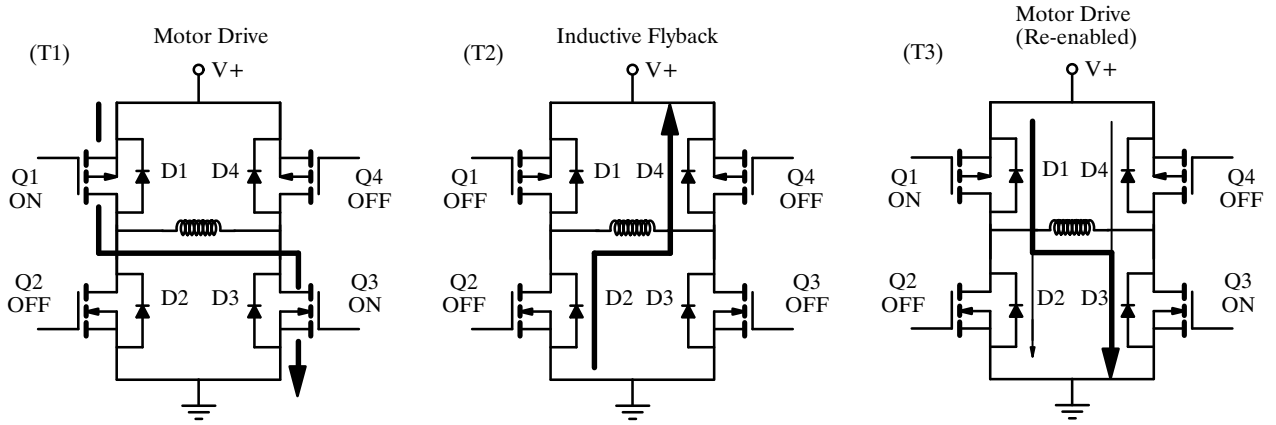
Driving Inductive Loads

When driving inductive loads with power MOSFETs, several parameters that might otherwise be of secondary concern become very important. One characteristic of inductive loads is flyback energy. When inductor drive current is interrupted, damaging flyback voltages can result unless diodes are used to clamp the voltage and allow the inductive flyback current to freewheel. Each power MOSFET contains a fast-recovery intrinsic diode that can be used as a reliable and efficient clamp for inductive flyback energy. Of particular importance in the use of the MOSFET's reverse characteristics are its intrinsic diode specifications—V_{SD} (reverse source-drain voltage, which is the diode forward voltage drop) and t_{rr} (reverse-recovery time).

The flyback current recirculating through the diode clamps is equal to the motor current, which reaches its maximum level during motor acceleration or braking. Although power lost in the clamp diodes (V_{SD} times the recirculation current) occupies a small percentage of the duty cycle, it can contribute significantly to overall MOSFET heating if the forward voltage drop is excessive. Both the n-channel and p-channel devices of each half-bridge are specified with a maximum forward voltage drop of 1.6 V at the MOSFETs' maximum (continuous) forward drain current rating.

The intrinsic diode t_{rr} becomes important any time the motor current is interrupted by turning off the MOSFET switches. When drive is re-enabled in the same path, while flyback current is still recirculating in the opposing clamp diodes, recombination will have to occur before the diode recovers and blocks voltage (Figure 2).

Figure 3 illustrates the relationship of the diode reverse-recovery characteristics with gate drive impedance. The load inductance is shown referenced to V+, and the upper MOSFET's gate is shorted to the source to isolate its intrinsic diode for demonstration purposes.



(T1) Q1 and Q3 ON for motor drive.

(T2) Power MOSFETs OFF, inductor flyback is conducted through diodes D2 and D4.

(T3) If Q1 or Q3 are turned on before the flyback energy is fully dissipated, a current path will exist between the power supply and the ground during the diode t_{rr}. The amount of shoot-through current that results depends on series gate drive impedance (how fast the opposing LITTLE FOOT device is turned on), stray series inductance, and diode reverse recovery time.

Figure 2. Clamping Inductive Flyback Energy

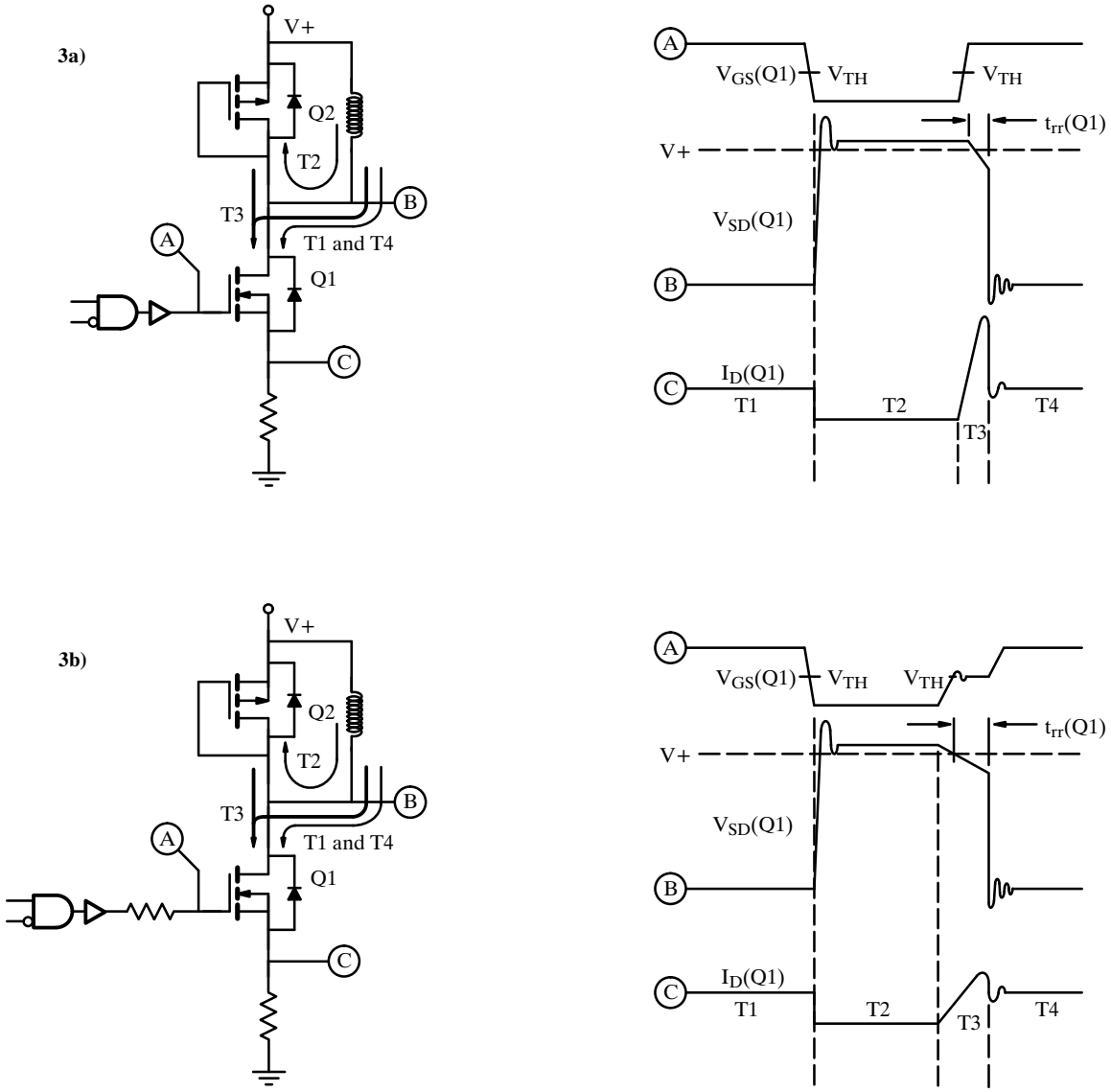
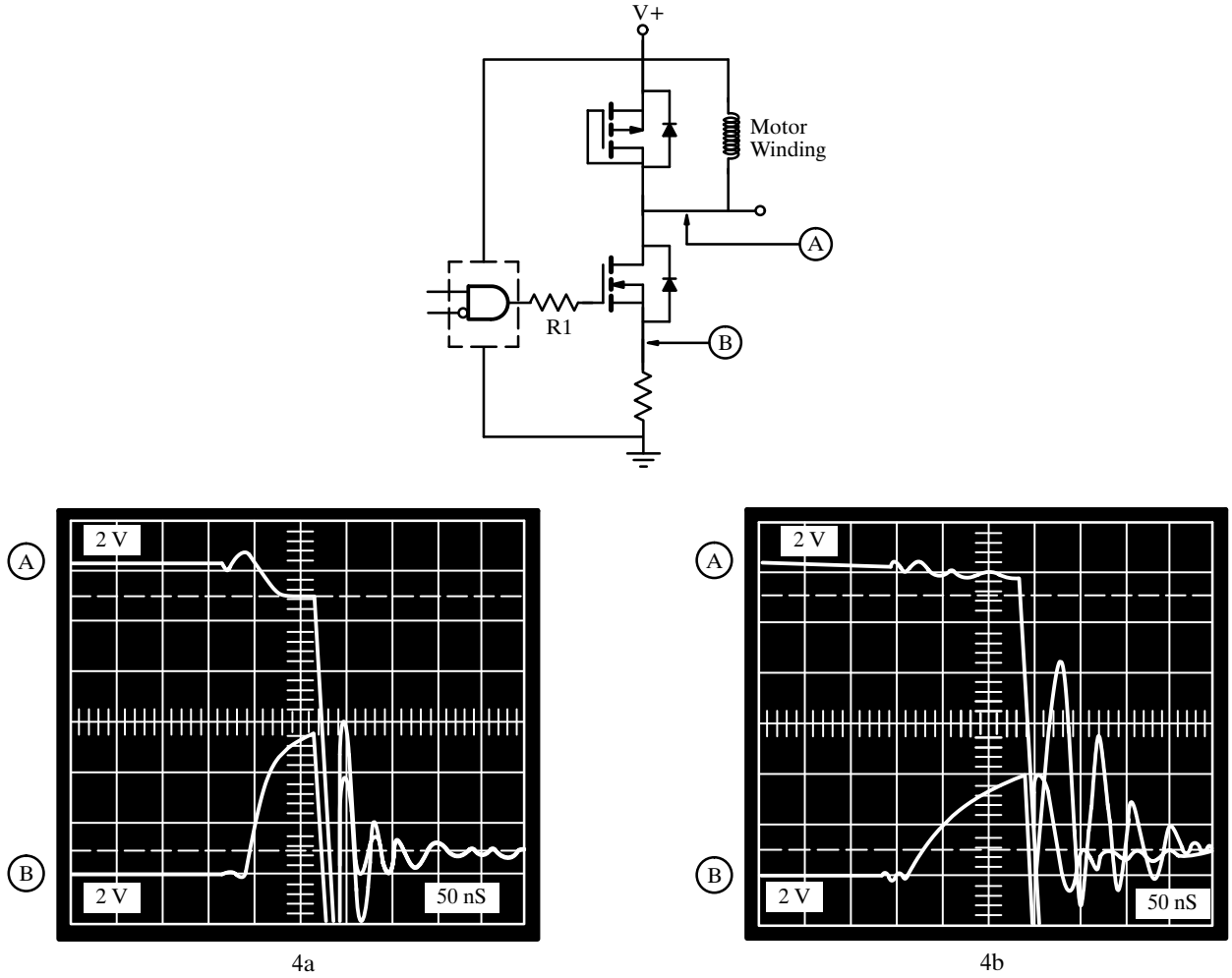


Figure 3. Shoot-Through Current and dv/dt vs. Gate Drive Impedance

During time T1, the lower MOSFET (Q1) is turned on and load current is conducted through the inductor to ground. At the leading edge of time T2, Q1 is turned off and flyback current from the inductor recirculates through the intrinsic diode in MOSFET Q2. Shoot-through current occurs during time T3, when Q1 is switched back on. As Q1 is turned back on, it conducts current from both the load and reverse current through the diode of Q2, which has yet to recover. When enough current is conducted to reverse the voltage potential across the diode of Q2, it begins to recover. Duration of the current spike is dependent on the power MOSFET t_{rr} (a function of the diode's forward current and forced recovery di/dt). The current spike magnitude depends on the product of the gate voltage and the g_{fs} of Q1 at the time of Q2's diode recovery (Figure 3a).

As the value of gate drive resistance (R1) is increased, the turn-on rate of Q1 (during time T3) is reduced (Figure 3b). By reducing the rate of gate drive voltage rise (dv_{GS}/dt), the level of gate voltage present when the diode recovers is reduced, thereby reducing the peak shoot-through current level. As gate drive impedance R1 is increased, the forced recovery current rate (di/dt) is also reduced, which actually increases t_{rr} in MOSFET Q2's diode. (The total amount of charge which must recombine remains the same regardless of di/dt, and since the maximum current level is now restricted, time is increased.) Efficiency is not increased by reducing peak shoot-through current, however, potentially damaging levels of peak current will be avoided, and EMI/RFI will be reduced.

Determining the proper gate drive impedance to achieve the desired reverse-recovery characteristics and system EMI/RFI requirements must be balanced against the maximum transition times required to achieve acceptable switching losses. As a basis for understanding the impact of switching time and the resulting switching losses on overall system efficiency, we must assume some typical operating conditions. If the modulation frequency is 20 kHz, one cycle will be 50 µs. If the transition time objectives are arbitrarily set at 1% of the overall duty cycle duration (500 ns total), each transition (including worst-case t_{rr}) must be less than 250 ns. The oscilloscope photograph (Figure 4a) demonstrates that this is a reasonable goal. These transition waveforms result when the configuration shown in Figure 4 is driven directly by a CMOS logic gate. The oscilloscope photograph in Figure 4b illustrates the output current and voltage waveforms with a 500-Ω series gate resistor (R1). In both examples, Figures 4a and 4b, a CD4000 series CMOS logic device was used to drive the power MOSFET gate.



4a 4b

Figure 4. CMOS Gate Drive and Resulting Output Waveforms (Si9942)

Aside from the obvious reasons for limiting di/dt during t_{rr}, extreme rates of dv_{DS}/dt can result at the end of time T3 (Figures 3a and 3b). This recovery dv_{DS}/dt (commutating dv/dt) is primarily a function of the di/dt and peak shoot-through current forced during the diode recovery time. All power MOSFETs have some sensitivity to commutating dv/dt; Figure 5 indicates what characterization data has shown to be "safe" dv/dt rates as a function of forward diode current prior to a forced recovery. This applies only if the forced voltage across the device (V+ or $V_{Battery}$) is above 85% of the $V_{(BR)DSS}$. For modern DMOS geometries, commutating dv/dt sensitivity decreases drastically and ceases to have any effect below approximately 60% of the $V_{(BR)DSS}$ rating.

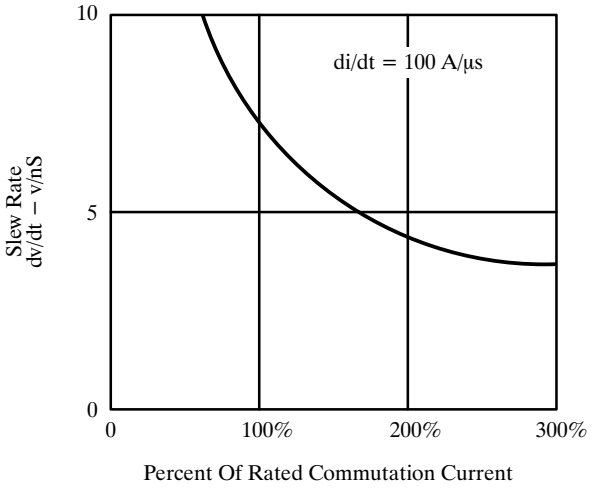


Figure 5. Reverse-Recovery dv_{DS}/dt Sensitivity

Common Gate Drive

A common cause of simultaneous conduction results from connecting the p-channel and n-channel gates together and driving them from a common logic signal. While this may be a completely acceptable gate drive method for capacitive loads or for lower voltage systems, it will probably result in excessive crossover current when driving inductive loads with 12 V across the bridge. If the gates are driven in common, the correct output states will result; however, this occurs at the expense of a current spike caused by both devices being partially turned on as the common gate voltage is in transition between approximately 2 V (n-channel threshold voltage) and 8 V (12 V minus p-channel threshold voltage).

Figure 6 demonstrates the crossover current that can exist in the Si9942DY at V+ = +12 V with the gates driven by a ramp voltage.

In this example, the crossover current reached a peak of 3 A, limited only by the g_{fs} of each device (with limited enhancement voltage above the threshold voltage) and by the series resistance.

In Figure 7, a pre-driver stage has been added that virtually eliminates crossover current under these same conditions. The impedance of the p-channel and n-channel buffer stage governs the turn-off times of the output devices. And R1, plus the buffer MOSFET's on-resistance, sets the turn-on times.

As will be discussed under "Driving Capacitive Loads," it may be perfectly acceptable to tie the gates together when driving capacitive loads.

Disk Drive Applications

Using dual MOSFETs with p-channel and n-channel devices allows the simplest gate drive circuitry to be used, since both gates can be pulled to ground or to the 12-V supply. The half-bridge used to drive each phase of the spindle motor (Figure 8) or head actuator (Figure 9) is typically driven directly by the output of a standard CMOS logic device powered from the same 12-V supply. While the relatively high output impedance of a CMOS logic device will not drive the capacitive gates of the half-bridge hard enough to attain maximum switching speeds, the combination will provide sufficiently fast transition rates to result in tolerable switching losses. Driving the power MOSFET gates with lower impedance drivers will result in faster transition rates and further reduce switching losses; however, the designer is usually forced to strike a balance between switching losses and increased EMI/RFI. This is of particular concern in rotating disk drive memories.

The 12-V supply provided to the peripheral function by the host computer system is usually clean and regulated to ±10%. One of the designer's greatest tasks is to achieve the desired motor drive performance without destroying the supply's integrity. This is accomplished by managing a number of trade-offs, such as the balance previously noted between transition rates and EMI. Another prime concern is any shoot-through current caused by the simultaneous conduction of both devices in one half-bridge. One common cause of this condition is the reverse conduction of current through the body-drain diode during the diode t_{rr}, as previously discussed.

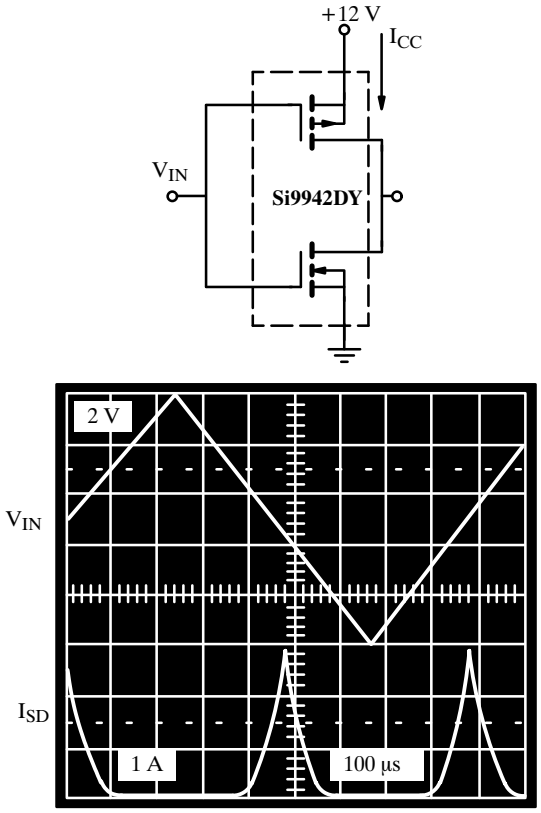


Figure 6. Crossover Current Caused by Common Gate Drive

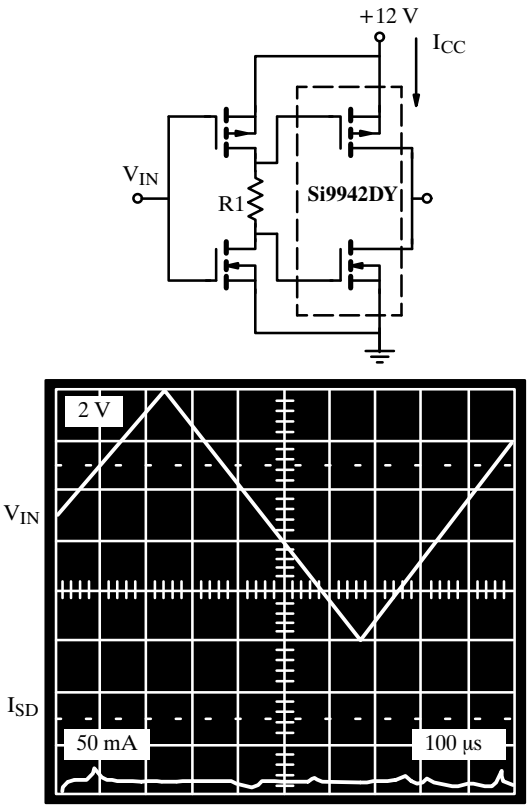


Figure 7. Complementary Buffer Stage with Shoot-Through Current Limiting

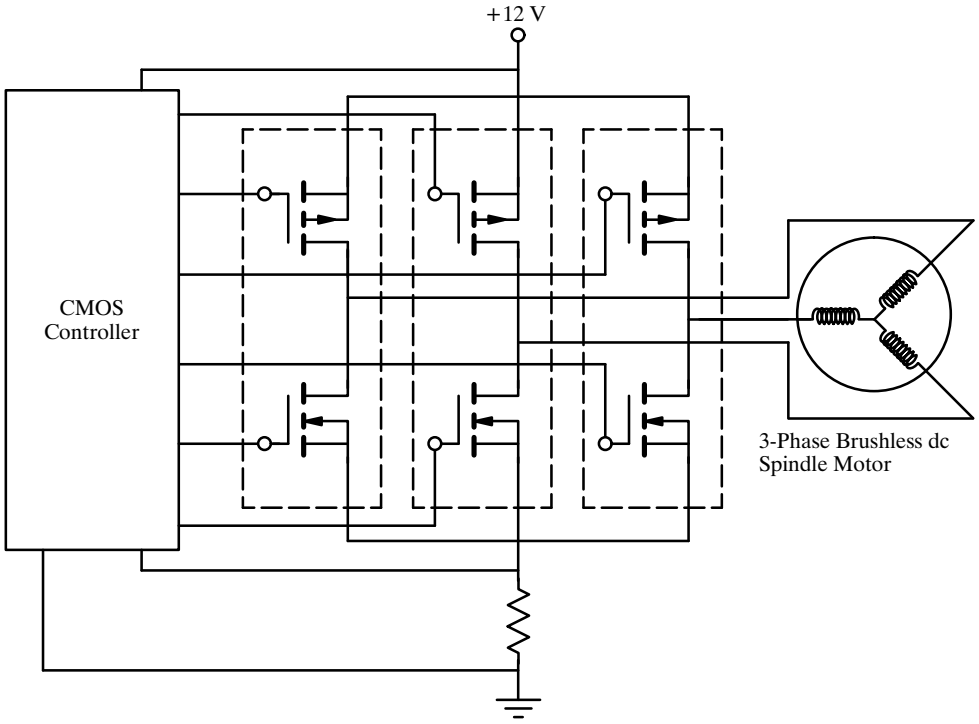


Figure 8. 12-V, 3-Phase Permanent Magnet Brushless Motor Drive

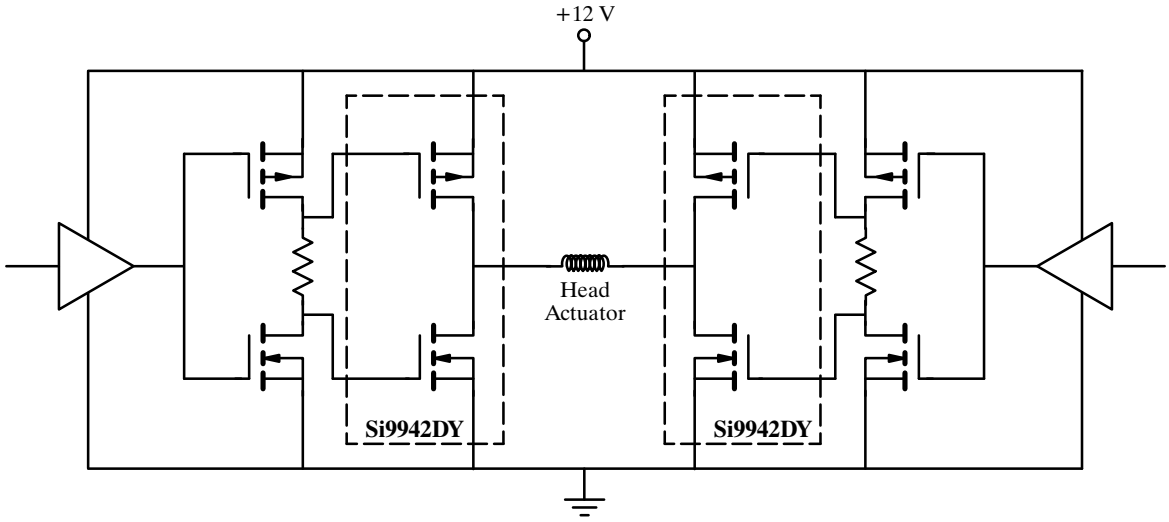


Figure 9. 12-V H-Bridge Actuator Drive

Driving Capacitive Loads

Highly efficient CMOS devices are a natural complement to the low-loss power handling capabilities of power MOSFETs. However, CMOS outputs are relatively high impedance and power MOSFET gates are highly capacitive. If high frequencies are necessary, some type of gate drive buffer must be used. The Si9942DY will function perfectly in this application as a very low-impedance, complementary output stage for the CMOS device. The gate capacitances are easily driven by standard CMOS outputs, and the single-stage, complementary pair adds minimal delay.

The high-efficiency CMOS current-mode regulator illustrated in Figure 10 demonstrates a combination that takes advantage of the characteristics of each device. The Siliconix Si9100 series of current-mode controller ICs, built with CMOS/DMOS (power IC) technology, includes regulators and controllers. The regulators feature an on-board output power device, and the controllers have a CMOS output designed to drive an external power MOSFET with higher current or voltage capability. This CMOS output is capable of driving power MOSFETs up to 1000 pF (C_{iss}) at the 500-kHz maximum switching frequency.

In the oscilloscope photograph in Figure 10, voltage waveforms demonstrate the rise and fall times attained at the common gates of the Si9942DY (Trace A) and the gate of the SMW14N50F output device used in this example (Trace B). Symmetrical rise and fall times of less than 10 ns are sufficient to provide minimal transition losses, even at 500 kHz.

With a capacitive load (Figure 11), the gates of the p-channel and n-channel complementary stage devices can usually be tied together and driven in common without the penalty of cross-conduction current that could be present with an inductive load. As discussed in the “Driving Inductive Loads” section, with 12 V across the complementary stage, both devices will be partially on as the gates’ transition between about 2 and 8 V. But with the capacitive load representing an essentially vertical load line during the first few nanoseconds of the transition, dv_{GS}/dt usually exceeds dv_{DS}/dt, and what would have been cross-conduction current goes into charging the load.

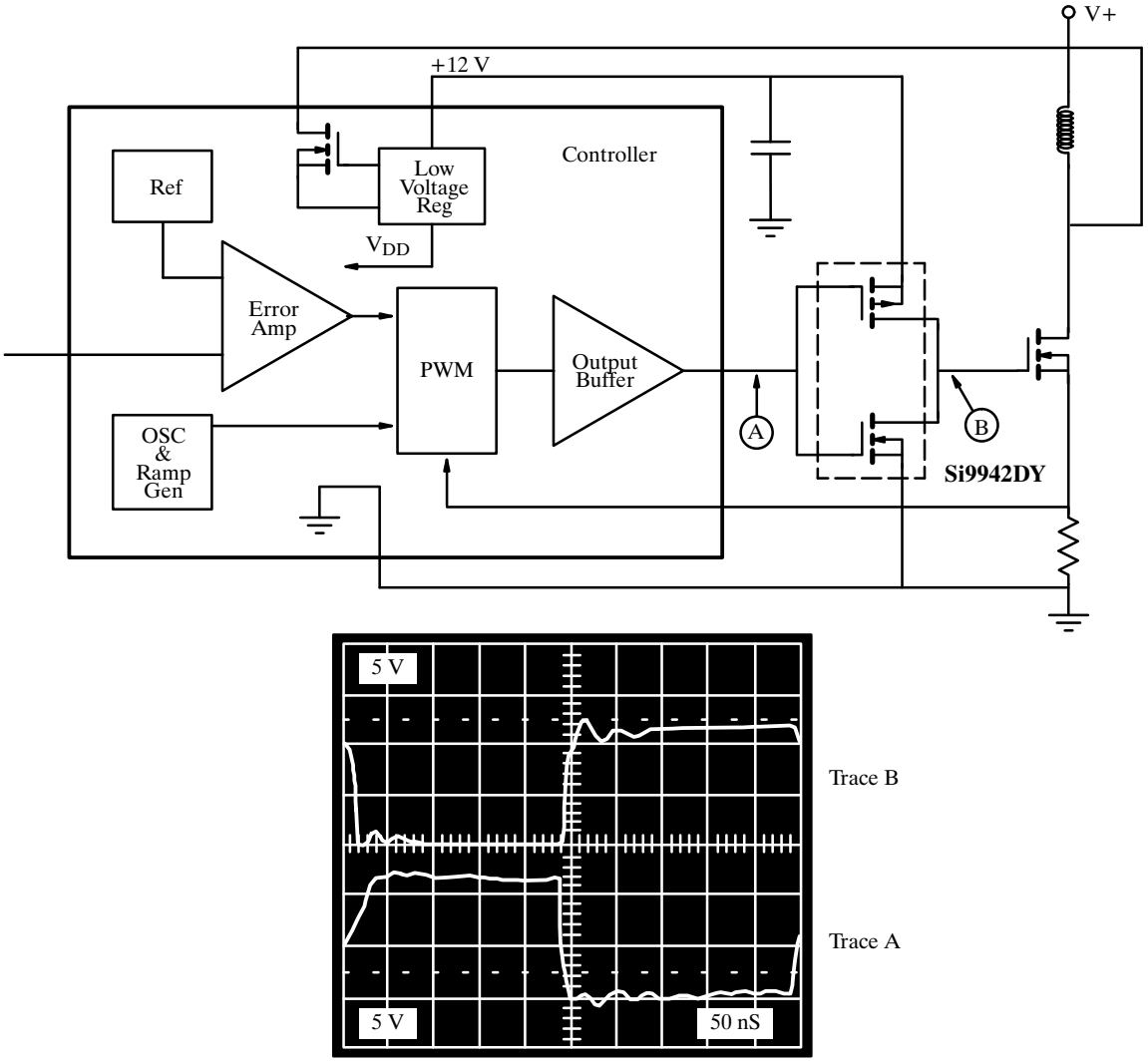


Figure 10. Very Low-Impedance Power MOSFET Gate Driver

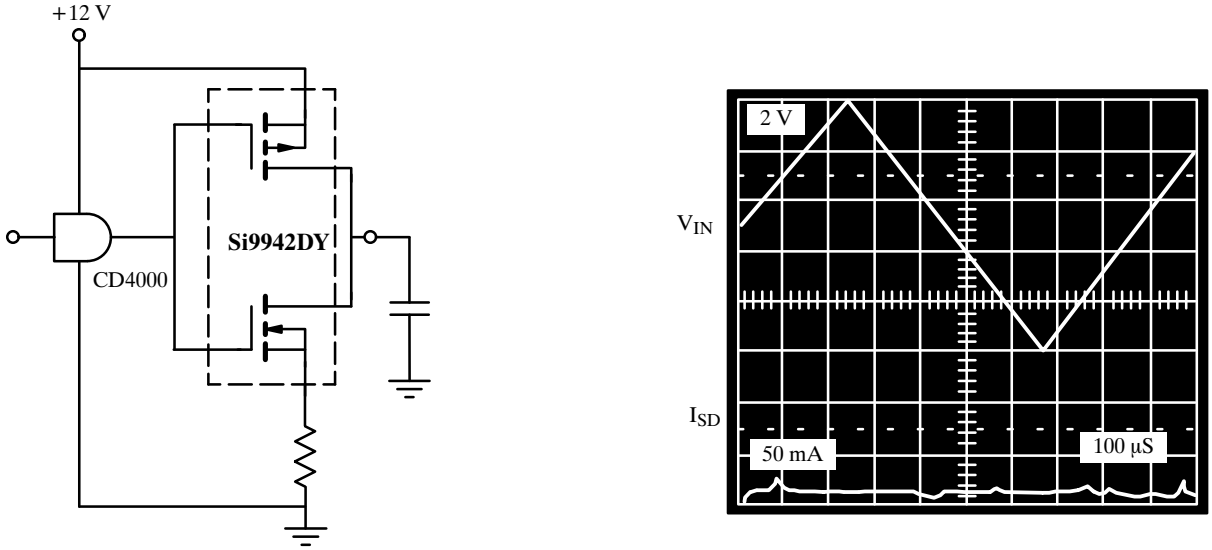


Figure 11. Common Gate Drive with Capacitive Loads

Summary

The Si9942DY combines p-channel and n-channel half-bridge architecture with the high-impedance gate characteristics of power MOSFETs, making the device extremely easy and efficient to drive. Rugged LITTLE FOOT devices are designed to provide reliable, optimized performance for inductive loads such as motors, actuators, and solenoids. The power MOSFETs' intrinsic diodes are designed and specified to function reliably and efficiently as clamp diodes when driving inductive loads.

The Si9942DY can also serve as a very low-impedance output buffer stage to extend the range of capacitive loads driven by CMOS circuitry. The p-channel and n-channel half-bridge configuration allows the two gates to be tied together and driven directly by a common CMOS output in low-voltage applications. The single complementary stage offers minimum propagation delay and very low-impedance output, which greatly extends the output power range of high-frequency CMOS controllers.